Electroplated Magnetics Open Door To Widespread Integrated Power

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At the recent Power-Supply-on-Chip (PwrSoC) Corridor Webinar 2020, EnaChip, a startup company specializing in the design and process development of micro-magnetic components on silicon substrates,[1] revealed the commercialization of their integrated micro-magnetic technology platform. Their simplified wafer processing coupled with a proprietary magnetic alloy enables smaller power inductors and transformers. Processors, system-on-chip (SoC) assemblies, sensors, multichip (heterogeneous) electronics can integrate these wafer-level magnetics to increase functional density and proximity, resulting in higher efficiency.

Breaking the barriers of high-frequency magnetics' performance at top efficiency, wafer-processing-cost, and scalable power level, EnaChip views their market as covering a broad range of integrated magnetics applications. These power applications include switching power sources for voltage regulation (for example, in processors and PMICs), for current regulation (such as in LED drivers) and for IoT, IIoT, and 5G systems.

But beyond these, there are a wide range of possible applications for integrated magnetics including wireless power; energy harvesting; low-signal conditioning; actuators for isolated switches; magnetic sensors, including the power section; automotive power and sensor electronics; medical applications—point of care devices (e.g., lab on chip), operational, and implanted electronics; and EMI suppression beads and RF antennas.

In this article we review the existing options for wafer-level integrated magnetics, discuss their limitations, and explain how EnaChip's multilayer electroplated core magnetics overcome these limitations.

Magnetic Thin Film Core Technology

A typical method for increasing magnetic density (compared to air core magnetics) is to stack layers of thin magnetic film on top of each other, separated by a thin insulating layer. If the magnetic passive is manufactured as part of the front end of line (FEOL) of a semiconductor manufacturing process, these stacks are created by sputtering magnetic material within a vacuum chamber.

Sputtering is a common form of physical vapor deposition (PVD). Its chief advantage is that the passive magnetic device can be manufactured on the same die as the rest of the semiconductor circuit. However, passives do not follow Moore's Law, so when the CMOS circuit scales down to a smaller node, the passives no longer effectively scale with the circuit. Consequently, these passives require additional and costly masks and process steps to add magnetic layers to make them compatible with the smaller process node.

Although sputtering thin film magnetics is technically feasible, this process is not commonly available at every semiconductor fab. Manufacturing costs, especially for thicker or taller stacks and available capacity, may limit market adoption.

Electroplating takes advantage of lower-cost manufacturing equipment and yields better performance depending on the magnetic material. The passive magnetic device can either be fully processed on a separate wafer to create standalone components or post-processed on the same wafer as the semiconductor circuit. Both scenarios reduce the parasitic effects associated with routing and interconnects.

Since this process is not tied to FEOL specific foundries, their performance is independent of process nodes. Table 1 shows the advantages and limitations of the three fundamental magnetic core technologies.

Table 1. Comparison of magnetic core technologies. (Source: EnaChip).

Air-Core	Multilayer Sputtered Core	Multilayered Electroplated Core
⇑ Easy to fabricate	⇑ High performance	⇑ Fast deposition
⇑ Low cost	⇑ Process/thickness control	⇑ Low-cost process
⇑ Low power loss	⇑ FEOL compatible	⇑ Intrinsically low stress
⇓ High near magnetic fields	⇓ Slow deposition rates	⇑ Low capital costs (BEOL-OSAT)
⇓ Low inductance	⇓ High-cost process	⇑ Highly scalable
⇓ Requires high switching frequency	⇓ High capital costs	⇓ Metallic high permeability μ crystalline films have low resistivity ρ → small skin depth → higher loss
	⇓ Thickness/stress limitations	⇓ Multilayer laminations needed for high currents
		⇓ Complex multilayer/multimask cost prohibited process

Traditional performance-footprint tradeoffs in wafer-level magnetics constitute a significant barrier to adoption and scale. Therefore, the industry needs a cost-effective, node-independent, high-throughput manufacturing method for magnetic passives. This method needs to be easily adopted by semiconductor companies enabling the next generation of power solutions. One solution is EnaChip's multilayer electroplated core magnetics.

EnaChip's president and founder, Trifon Liakopoulos, discloses, "EnaChip commercialized the electroplating multilayer magnetic core process. In parallel, we developed a thick electroplating copper technology. This process is compatible with the back-end-of-line (BEOL) fabs. That makes it independent of any semiconductor process either directly in a chiplet assembly or as a monolithic post-CMOS process in an outsourced semiconductor assembly and test (OSAT) wafer-level packaging assembly. The resulting magnetic passives address an extensive range of applications with low manufacturing costs."

"We mitigated multilayer electroplating core limitations with process and innovative material adaptations. We substantially simplified the electroplating manufacturing process by considerably reducing the number of steps and masks used. For example, fabrication of an eight-layer magnetic core can be done in five main process steps instead of 72 and by using a single mask instead of 16 masks. We are now ready to move to the next commercialization step," adds Liakopoulos. Table 2 identifies the electroplating core limitation overcome by EnaChip's technology.

Table 2. Electroplating limitation targets and EnaChip's mitigations (Source: EnaChip).

Electroplating core limitations	EnaChip's mitigations
⇓ Metallic high-permeability μ crystalline films have low resistivity ρ → small skin depth → higher loss	⇑ High-resistivity ρ and high-permeability μ proprietary alloy → increases performance up to 30 MHz
⇓ Multilayer laminations needed for high currents	⇑ Enachip's high saturation flux density alloy can accommodate higher values of current with less magnetic material
⇓ Complex multilayer/multi-mask cost prohibited process	⇑ Single-mask process for multiple magnetic layers

Matt Wilkowski, VP of Magnetics Technology & Engineering, explains, "Our initial products are targeting the current range of 1 A through 4 A. The inductance range is tens of nanohenries to hundreds of nanohenries, and footprints as small as 1.5 mm x 2.0 mm utilizing multilayer core stacks of 1-micron thru 3-micron thickness per magnetic layer. The target product roadmap is scalable to 10-A applications requiring lower values of inductance and dc resistance."

In addition to the single-mask fabrication process, EnaChip's proprietary magnetic alloy or EnaChip Alloy (ECA) reduces the required magnetic layers per nanohenry, further reducing manufacturing complexity and cost. ECA permits switching at a higher frequency. Inductor performance data is shown in the figure.

The EnaChip inductor is low loss, achieving very high efficiency at rated current up to 30 MHz, compared with NiFe with the same efficiency at a maximum of 4 MHz. The company claims that the ability to function efficiently at higher frequencies reduces the inductor size proportional to the frequency increase. Thick copper windings improve thermal performance and reduce micro-inductor dc power losses.

With this type of magnetics, designers will be able to take full advantage of wide-bandgap transistor performance. Will such magnetics eventually surpass 50 MHz, further reducing the inductor size?

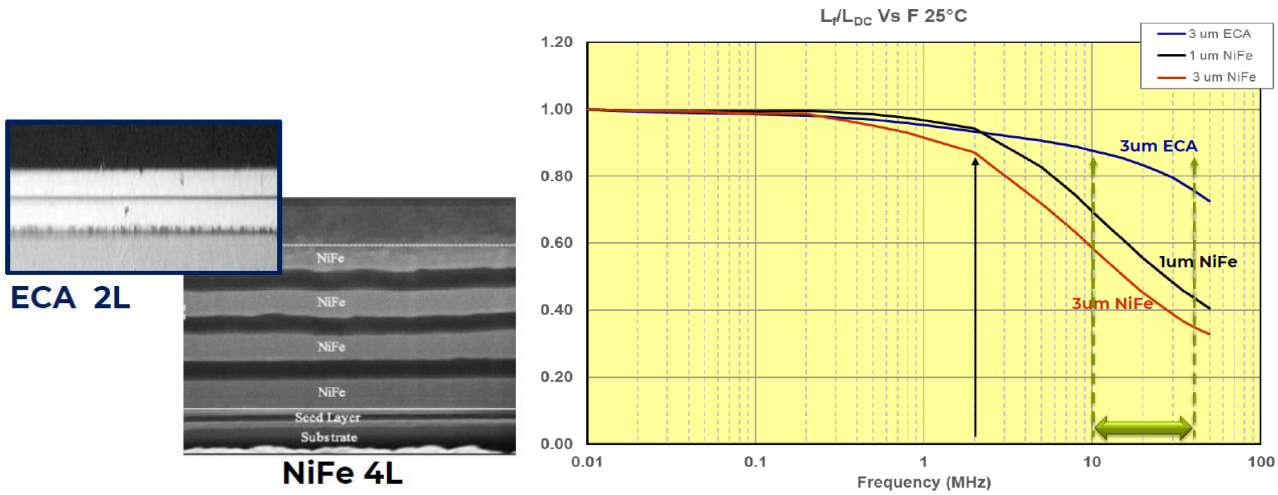

Figure. Two 3-µm ECA alloy layers vs. four 3-µm NiFe layers (Source: EnaChip).

EnaChip plans to partner with a select group of leading semiconductor foundries, outsourced semiconductor assembly and test (OSAT) companies, and component suppliers to fabricate wafer-level magnetics through technology license, including process design kits (PDKs) and design libraries. This multipath will lead to faster and broader adoption of Enachip's wafer-level magnetics technology while overcoming volume scale limitations typically associated with start-up companies.

The BEOL compatible wafer-level magnetic products are FEOL-process independent, allowing for multiple manufacturing options such as a) post-processing within the original fab, b) onshore or offshore OSAT or c) heterogeneous SoC fabricator. The portfolio product types include but are not limited to thick copper toroid micro-inductors, multilayer core toroids and solenoids, electromagnetic actuators, transformers, spiral coils and magnetic sensors.

Partnerships with large-scale volume manufacturing fabs will facilitate feasible commercialization of this ground-breaking manufacturing process. EnaChip's business model is a continuous progressive cycle that, through technology licensing to volume manufacturing fabs and adaptation from industry-leading customers, builds an integrated and vertical power ecosystem that benefits from fundamental cost-effective and scalable integrated magnetics technology.

References

1. EnaChip website.

2. "Commercialization Activities for Wafer Level Magnetics," by Trifon Liakopoulos, co-authored by Matt Wilkowski, Mark Allen, EnaChip, and Jun Beom Pyo, University of Pennsylvania, a PwrSoC Corridor Webinar 2020 presentation, November 2020 (available to the public in May 2021).

3. "Multiscale Nanolaminated Metallic Cores for High Frequency Magnetics," presented at the Power Sources Manufacturers Association (PSMA) High Frequency Magnetics Workshop, March 2019, by Mark Allen, University of Pennsylvania, co-authored by Jooncheol Kim, now with Samsung, and Minsoo Kim, now with Apple.

4. "Integrated Power – A Virtual Panel Session," a presentation at the IEEE/PELS Virtual Seminar October 2020, with speakers Steve Allen, pSemi (a Murata Company); Wonyoung Kim, Lion Semiconductor; Stephen Oliver, Navitas; Noah Sturken, Ferric; and Kirk Bresniker, HP Labs/H.P.E.

About The Authors

Arnold Alderman is the founder and president of Anagenesis, a technical marketing consultancy in Los Angeles, Calif. Arnold has been a presenter at, and an organizing member of the PSMA and IEEE/PELS sponsored PwrSoC Workshop series since 2008 and general chair in 2014. The PwrSoC Workshop assembles leading global technologists to present their progress in creating a commercially viable, completely integrated power converter.

Arnold is also a presenter and organizing member of the upcoming PSMA sponsored 3D Power Electronics Integration and Manufacturing (3D-PEIM) Symposium, covering heterogeneous integration. Anagenesis has recently published their 7th biennially PSiP & PwrSoC Market Report.

Arnold has 19 years of experience as a technical marketing consultant assisting companies from start-ups to major international conglomerates. His company Anagenesis combines both engineering and marketing skills to develop both commercial and client-specific market reports.

Arnold has 16 years of experience in product and strategic marketing at both Fairchild Semiconductor and International Rectifier. He also had 12 years prior experience in commercial power conversion equipment design, ranging from 2 W to 12 MVA, in a wide variety of power electronics applications. He holds an MBA from the University of New Haven in Connecticut and a BSEE from Northeastern University in Boston, Massachusetts. Arnold also holds four patents. He can be reached at arnold.alderman@anagenesis-inc.com.

Ada Cheng has extensive semiconductor and marketing expertise and experience. She has briefed many managers, sales professionals, and executives on various aspects of the semiconductor market. Cheng is currently a principal marketing consultant with AdaClock.

Prior to AdaClock, Ada was a senior corporate marketing manager at International Rectifier, and before that, a principal analyst with Gartner Dataquest covering the analog semiconductor market. Moreover, she has served as an invited member of the APEC conference committee as the OEM Initiative Chair. In addition, she is on the Power Sources Manufacturers Association (PSMA) board of directors since 2019, and she actively participates in the marketing, reliability, and energy management committees.

Before making her major career change into marketing, Ada had various engineering and project management roles at Motorola Semiconductor Products Sector (now Freescale Semiconductor and ON Semiconductor). Ada holds an MBA degree from Arizona State University and a BSEE degree from Carnegie Mellon University. She can be reached at ada@adaclock.com.

For more on power magnetics design and technology, see these How2Power's Power Magnetics section.