Micro-Magnetics Based on Single-Litho Core Laminations

Establishing a New PwrSoC Paradigm:

Higher Energy Density & Lower Power Losses for Cost Effective Wafer Level Magnetics

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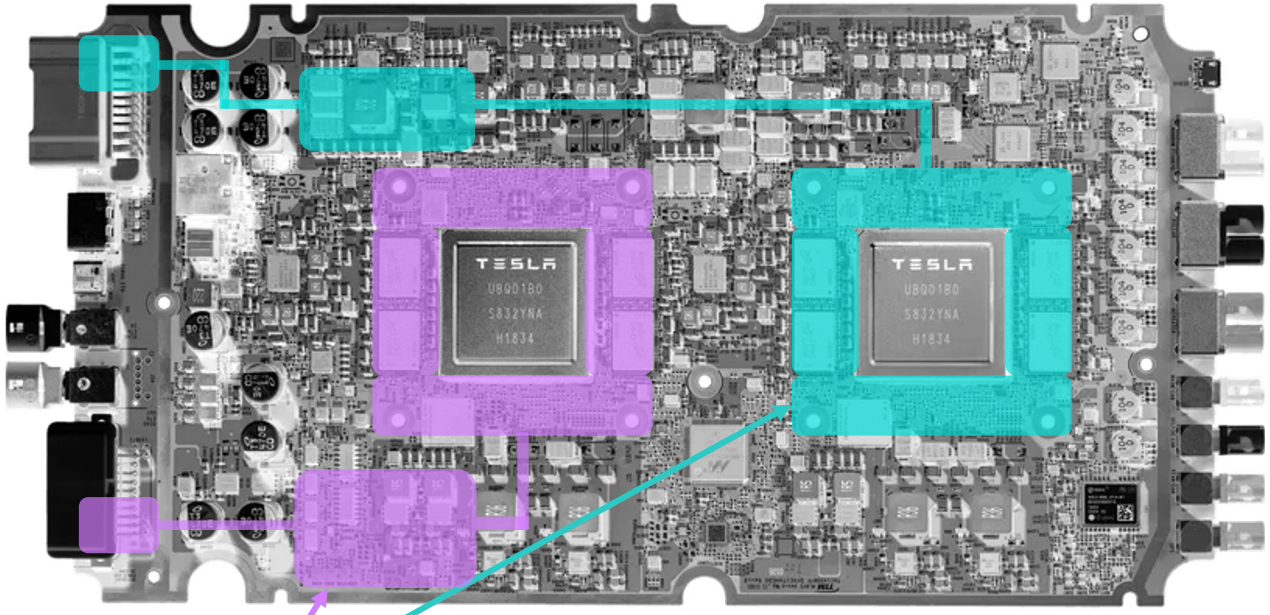
EnaChip Inc. – Intro

- Enachip *("One"-Chip) started operations in 2018 (early stage, VC funded startup)*
- *Mission: Re-invent Power Management by Commercializing Wafer Level Magnetics*

HQ Located between NYC and Philadelphia (30min south of Newark Airport)

THE POWER PROBLEM



Tesla AI dual redundancy AI computer

Power Is Wasteful And Uses Too Much Space

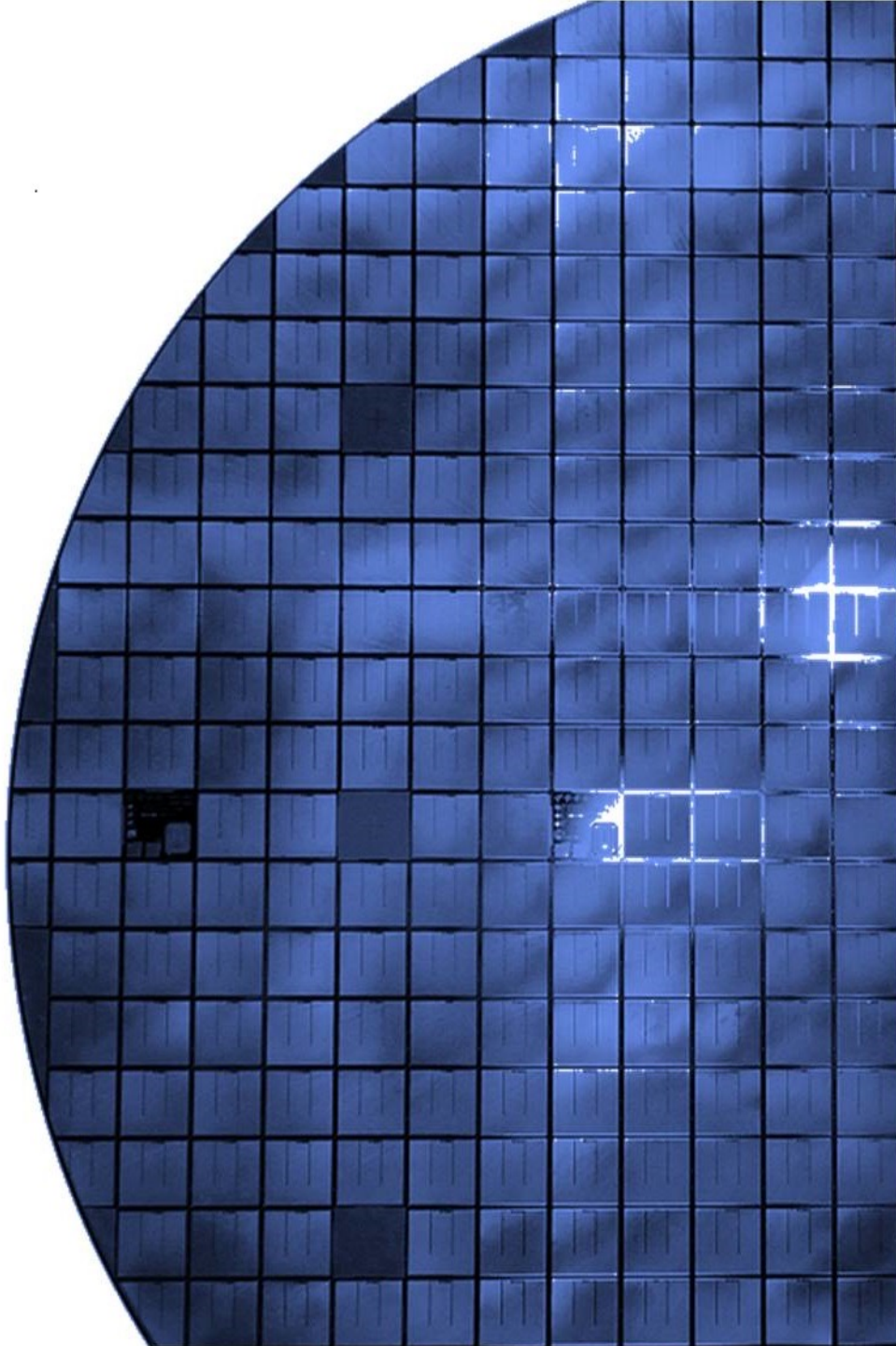
Example chipset

There are ***1600 I/O connections*** per processor

The majority of connections (***60%***) are for **Power**

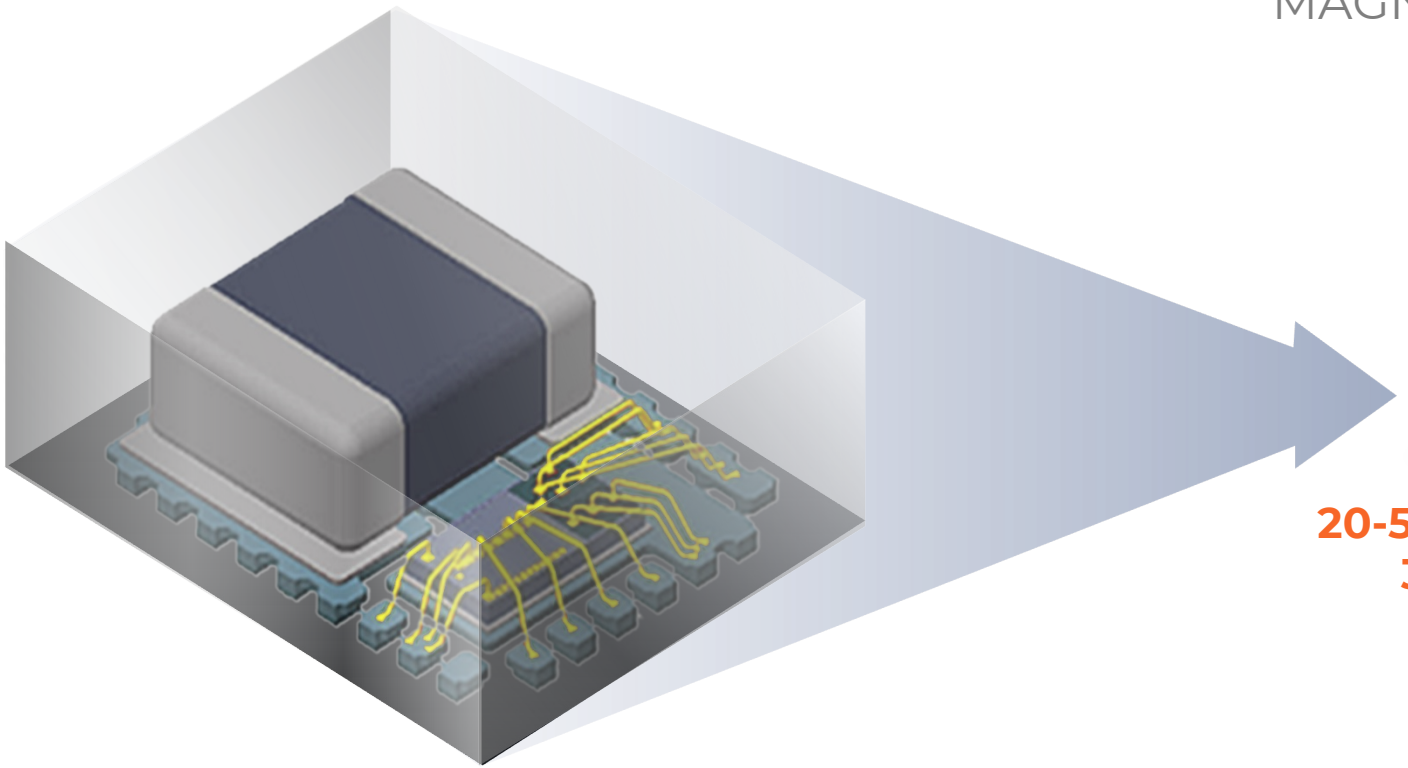
THE ROOT CAUSE of POWER INEFFICIENCIES

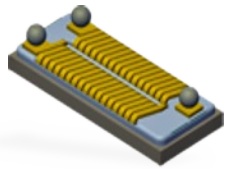
Power
Is Separate From
Silicon



EnaChip – Breakthrough Innovation in Integration

COMMERCIALLY VIABLE TECHNOLOGY THAT INTEGRATES POWER MAGNETICS WITH SILICON IC





20-50% Energy Savings
30x Smaller Size
3x Lower Cost

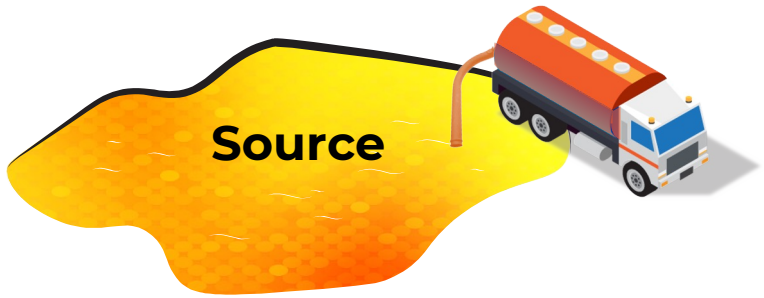
Power System in Package
State of the Art

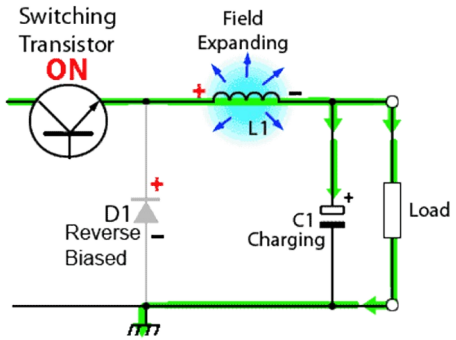
Power System on Chip
EnaChip Enabled Solution

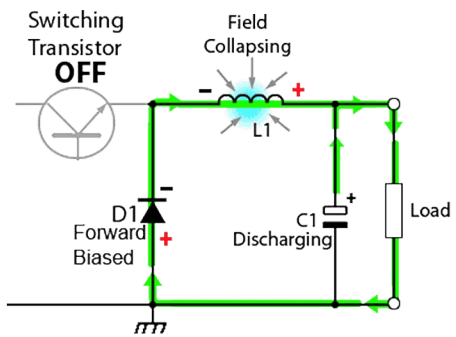
Wafer Level Magnetics

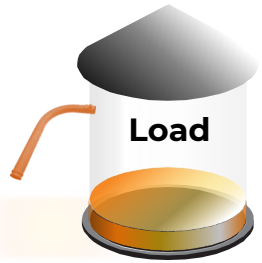
(Si & GaN trends to higher F_{sw} shift the PwrSoC's bottleneck to magnetics)

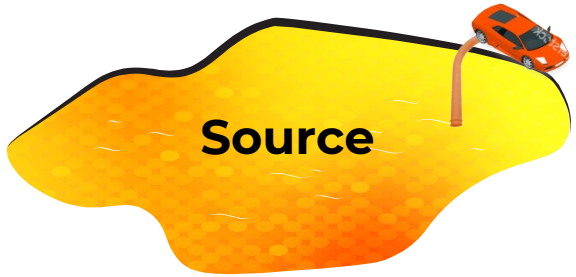
The inductor is acting as an energy storage element on a switching converter

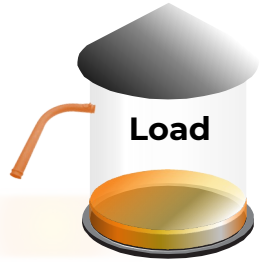










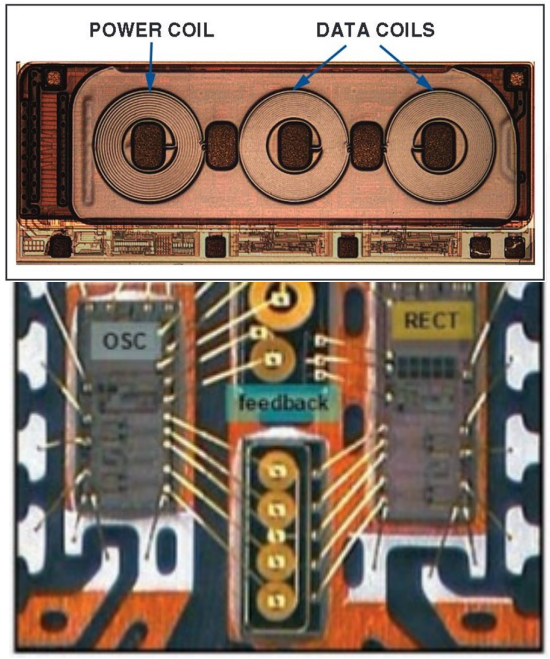


Inductor size reduction:

- Core Materials: High B_{sat} allows for size reduction
- Output Power: High F_{sw} allows for size reduction
- High F_{sw} increases system losses due to core material limitations and IC switching losses
- Multi-layered laminated cores required for meaningful integration of magnetics

Wafer Level Magnetics
(Core technology options)

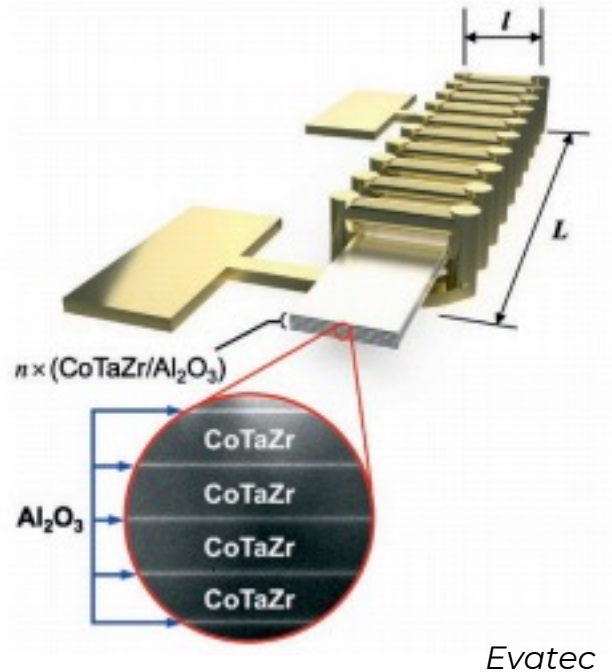
Aircore WLM



iCoupler, ADI

Electroplating windings

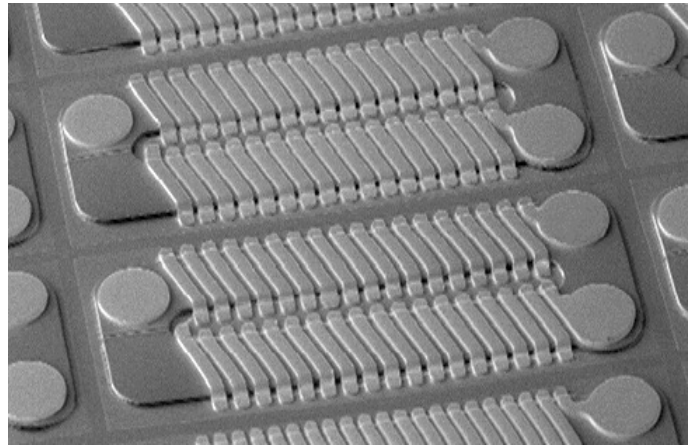
Multilayered thick film sputtered core



Evatec

Electroplating windings

Electroplating thick film core



Enpirion

Electroplating windings

Wafer Level Magnetics
(Core technology comparison)

Aircore WLM

- ⬆ Easy to fabricate
- ⬆ Low cost
- ⬆ Low power loss
- ⬇ High near magnetic fields
- ⬇ Low inductance
- ⬇ Requires high F_{sw}

Multilayered thick film sputtered core

- ⬆ High performance
- ⬆ Process/thickness control
- ⬆ FEOL compatible
- ⬇ Slow (.1µm/min)
- ⬇ High cost process (~10-20x of the plating)
- ⬇ High capital costs (>5X over electroplating)
- ⬇ Thickness/Stress limitations (<20L, <3 um)

Power ≈ core thickness

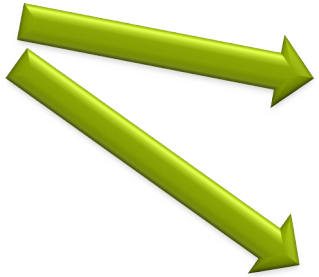
Electroplating thick film core

- ⬆ Fast deposition (1um/min)
- ⬆ Low cost process
- ⬆ Intrinsically low stress → No. layers (>100)
- ⬆ Low capital costs (BEOL-OSAT)
- ⬆ Highly scalable
- ⬇ Metallic high µ crystalline films have low ρ → small skin depth → higher loss
- ⬇ Multi-layer laminations needed for high currents >1A

Complex multi-layer/multi-mask **cost prohibited process**

Enachip's Technology Platform

Enachip addresses the electroplating core shortcomings to enable a high performance WLM cost competitive solution



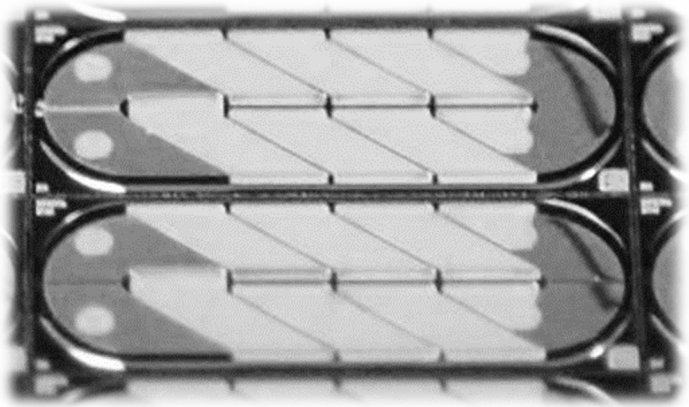
Electroplating core

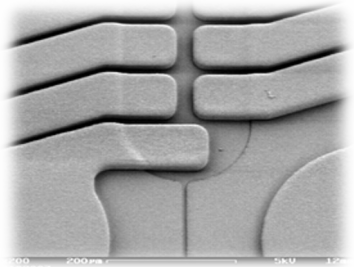
- ↑ Fast deposition process (1µm/min)
- ↑ Low cost process
- ↑ Intrinsically low stress → No. layers (>100)
- ↑ Low capital costs (BEOL-OSAT)
- ↑ Highly scalable
- ↓ Metallic high µ crystalline films have low ρ → small skin depth → higher loss
- ↓ Multi-layer laminations needed for high currents >1A

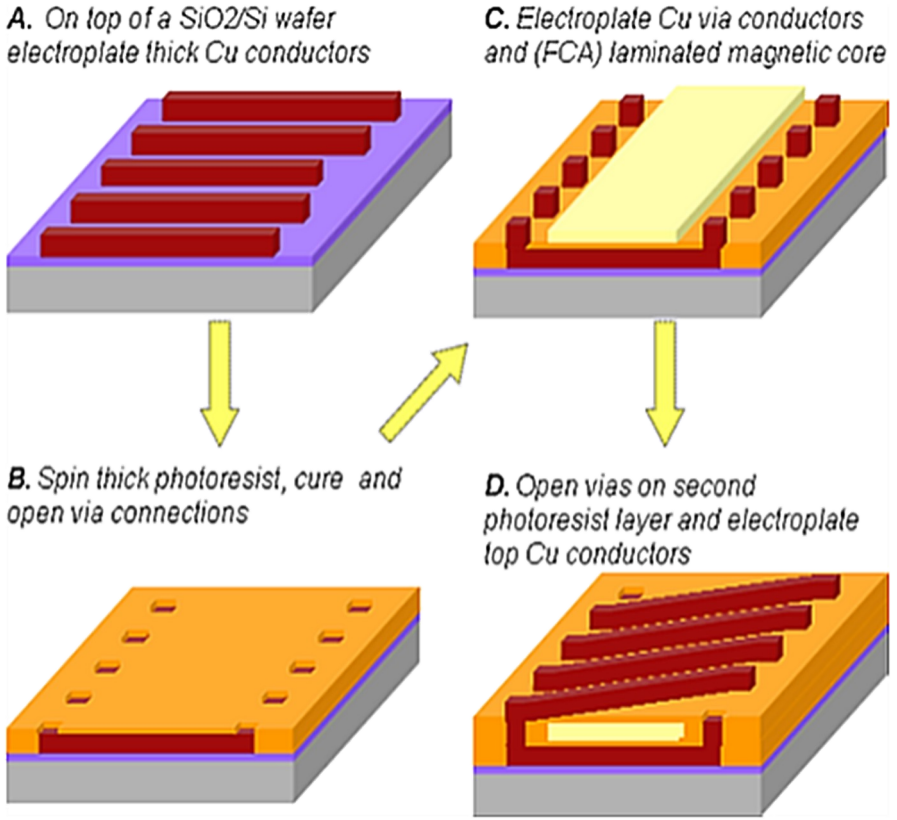
Complex multi-layer/multi-mask **cost prohibited process**

Key Process Modules
(Electroplated micro-coils)

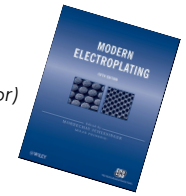
- Thick electroplated Cu (5um – 80um)
- Dielectric insulation/planarization
- Electroplated high frequency magnetic alloy laminations





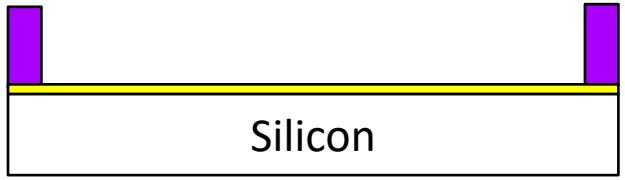


Ref. Modern Electroplating, 5th edition
Mordechay Schlesinger (Editor), Milan Paunovic (Editor)

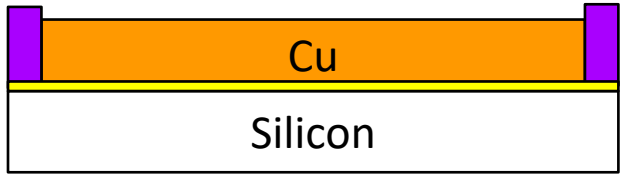


Process Flow

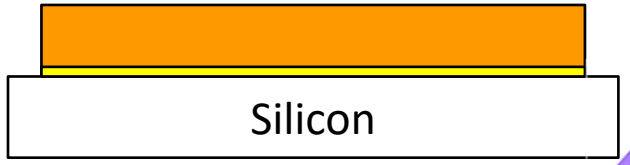
Seed



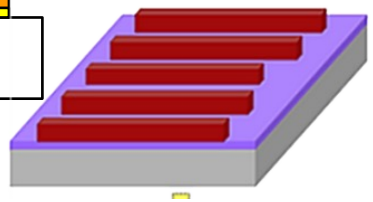
Litho

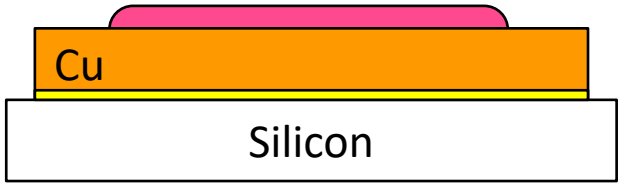


Cu

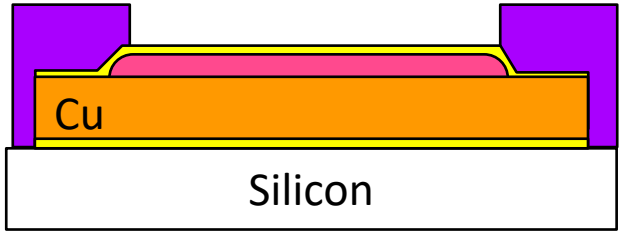


Etch seed

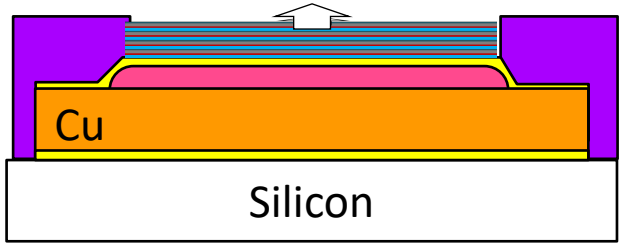




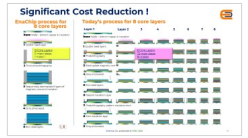
Litho/HCPR

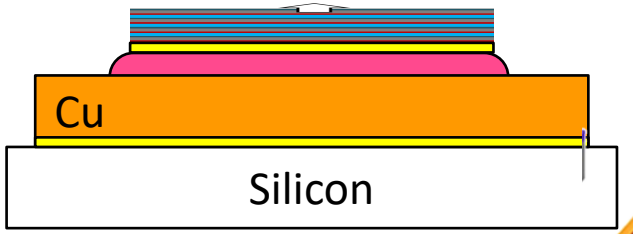


Seed/Litho

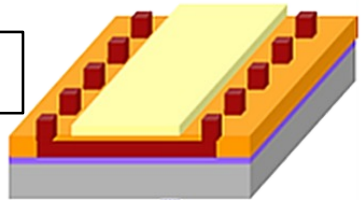


Multi ECA

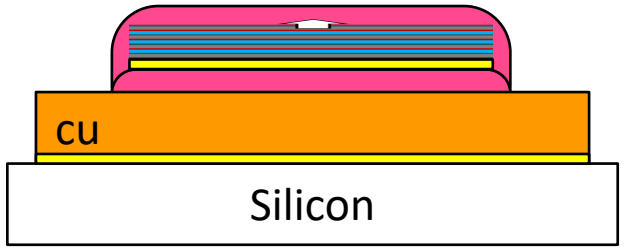




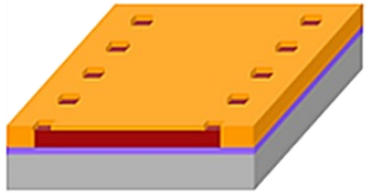
Strip/Etch seed

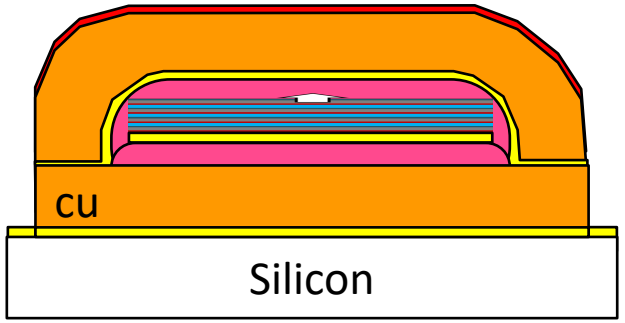


Process Flow

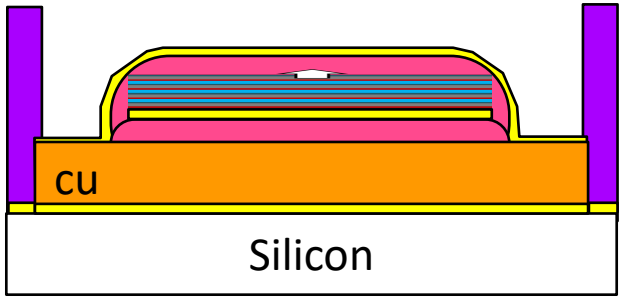


Litho/HC

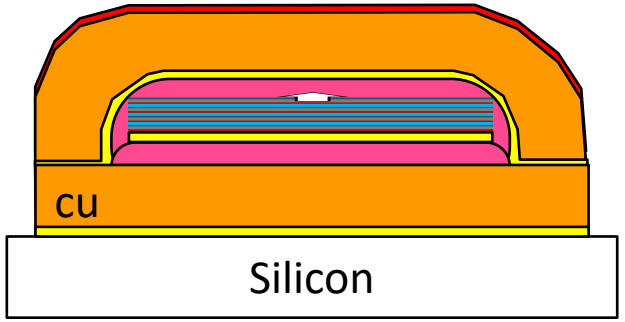




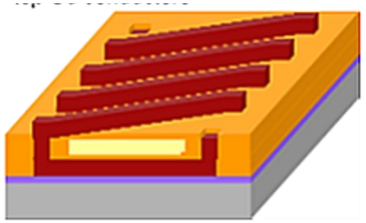
Strip PR



Seed/Litho



Etch Seed



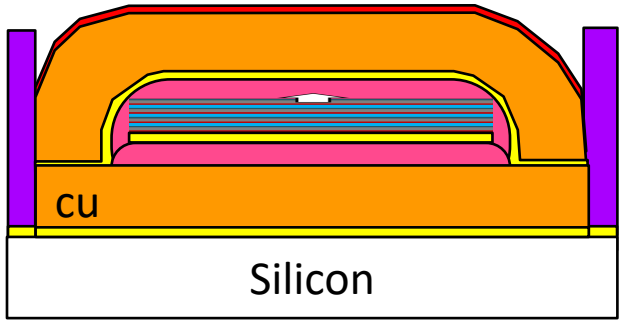
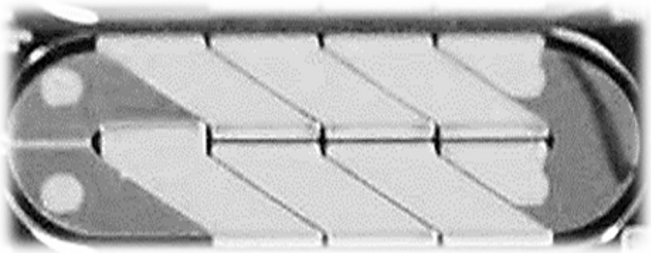


Plate Cu/Ni/Au



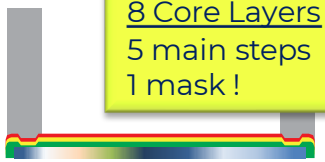
Significant Cost Reduction !

EnaChip process for 8 core layers

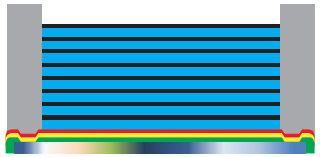
base Wafer - bottom copper & insulation

1 Sputter Seed Layer

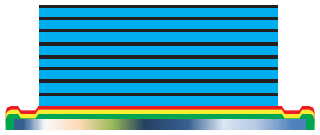
8 Core Layers
5 main steps
1 mask !



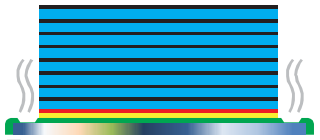
2 Thick photolithography



3 Sequentially electroplate 8 layers of magnetic core and insulation

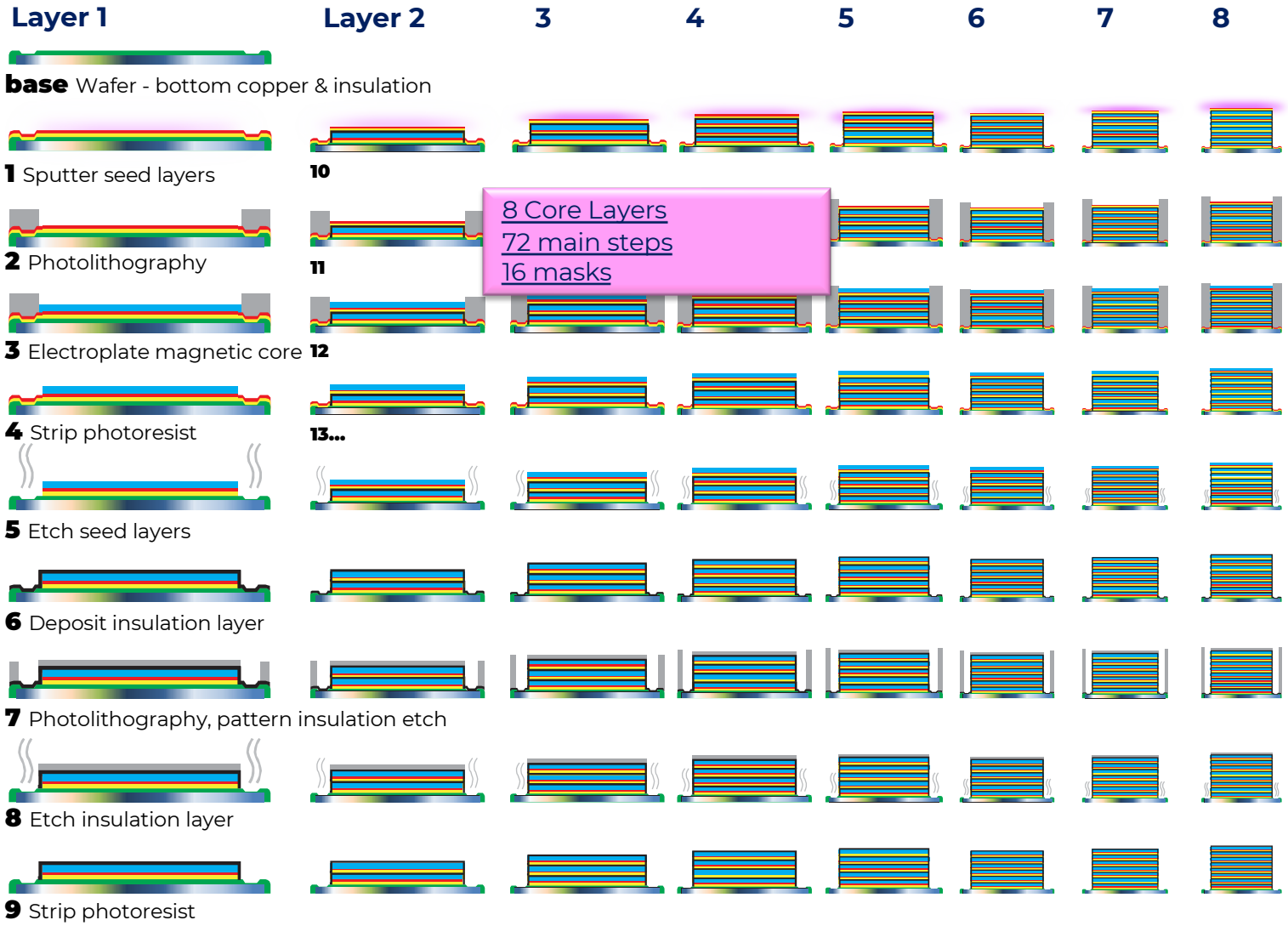


4 Strip photoresist



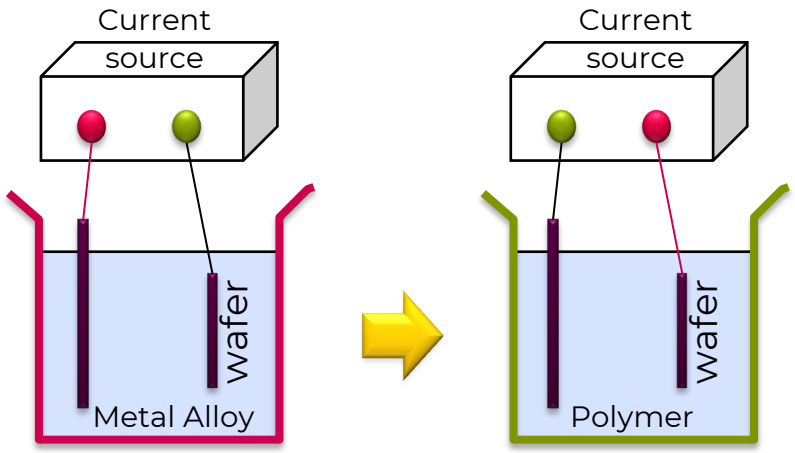
5 Etch seed layers

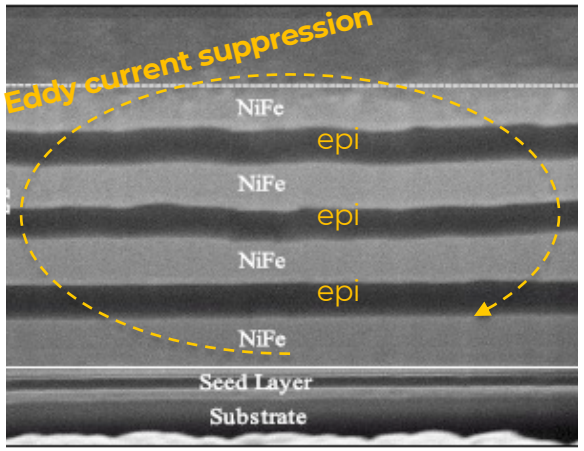
Today's process for 8 core layers

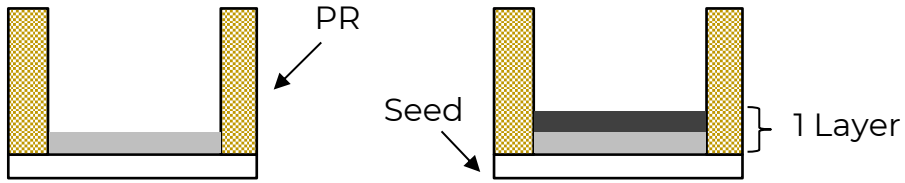


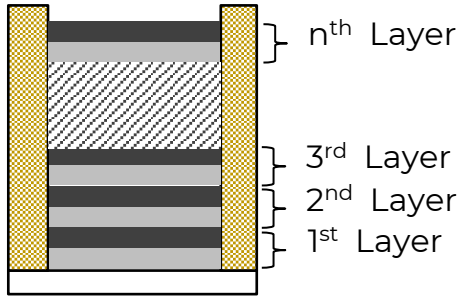
Multi Layer process incorporates electroplated insulator (epi)

- Electrochemically synthesized insulator
  - Conjugated polymer based
- Conductivity < 1S/m



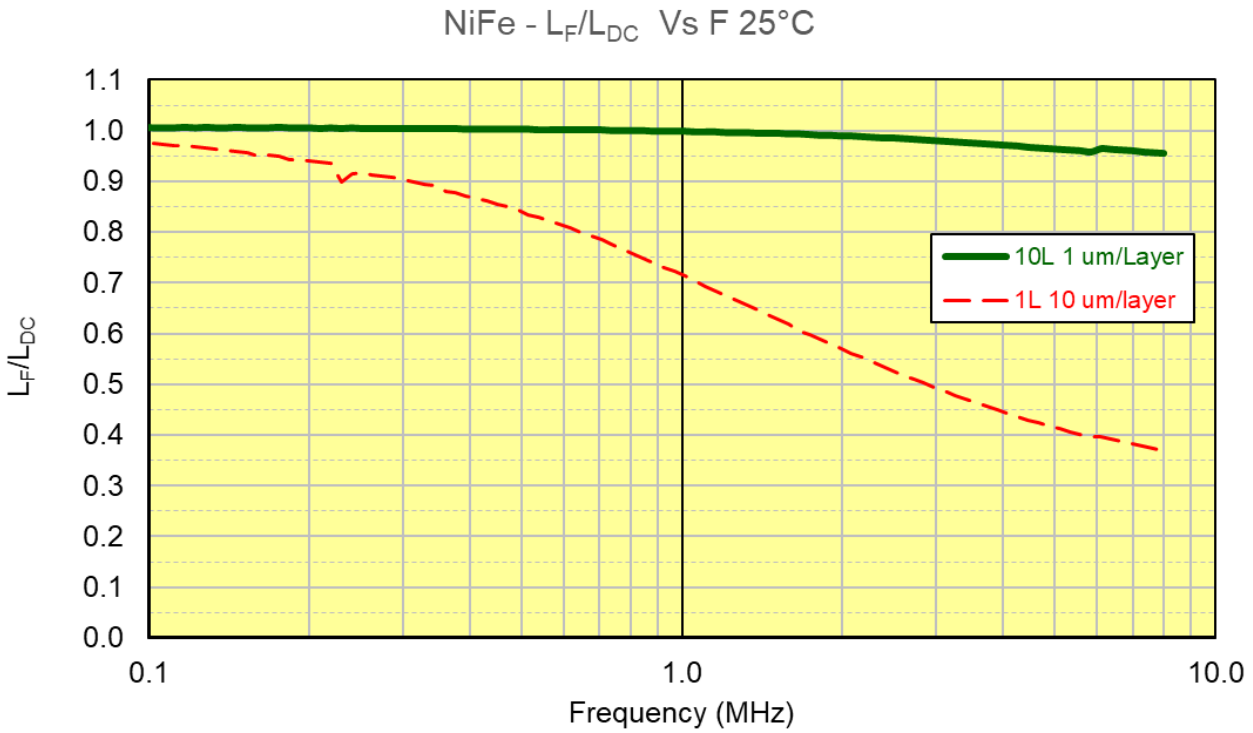


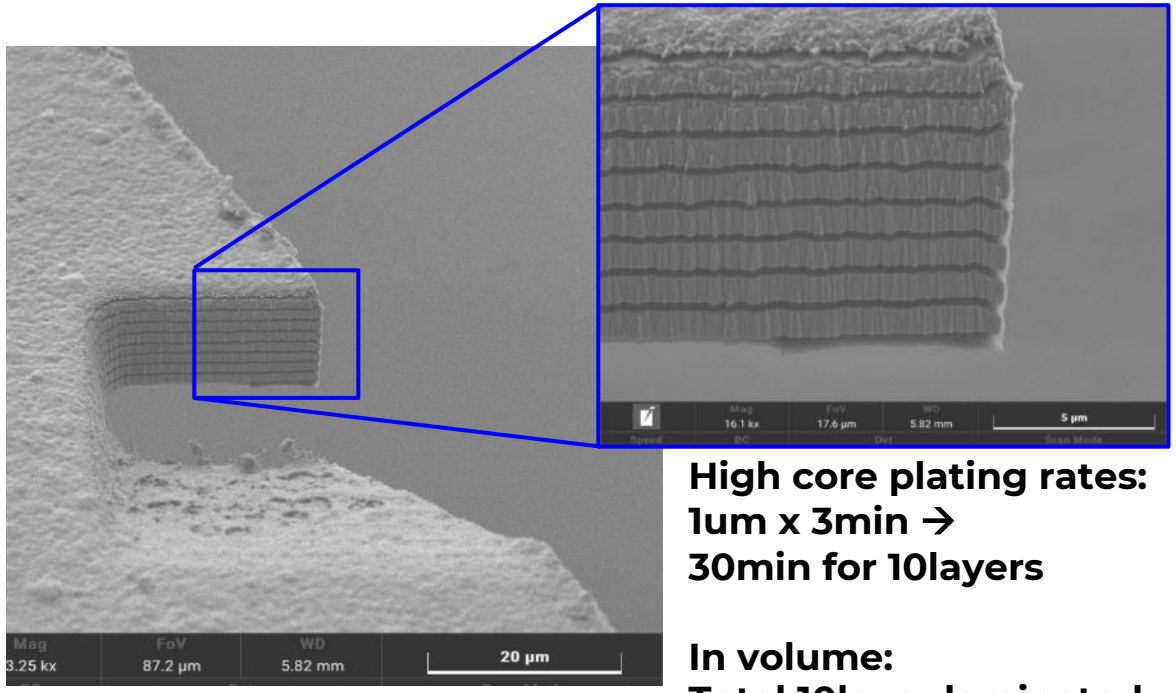




Multi Layer process Thin Insulator !

- Multiple layer with thin Insulator → Very high layer packing coefficient → Low profile cores
- EPI performance is comparable to ideal insulator with ability to suppress Eddy Current Loss

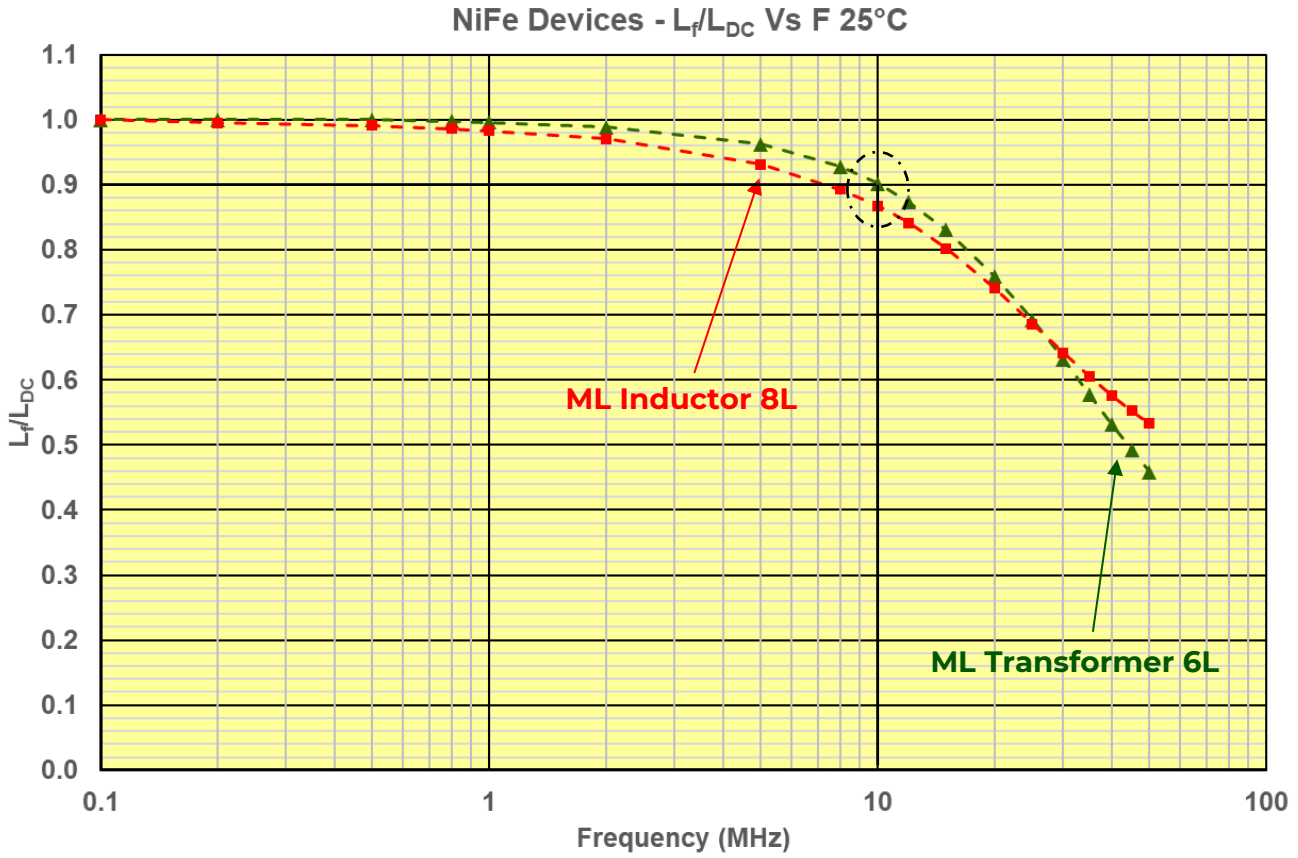




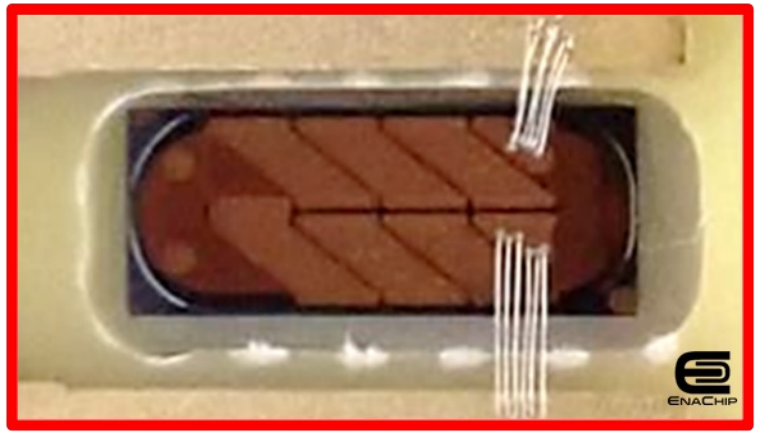
High core plating rates:
1um x 3min →
30min for 10layers

In volume:
Total 10layer laminated core process time: 1-2 hrs

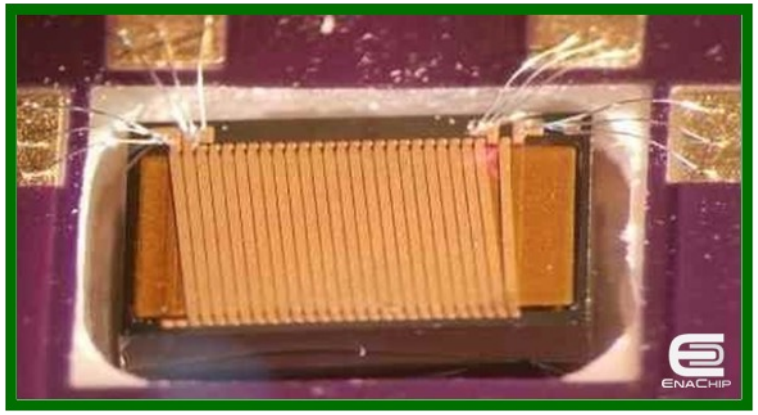
Device Performance
Using Mag Core with Single Mask n-Layer process



EnaChip multilayer process extends the performance of NiFe materials to maintain higher values of inductance at higher frequencies.

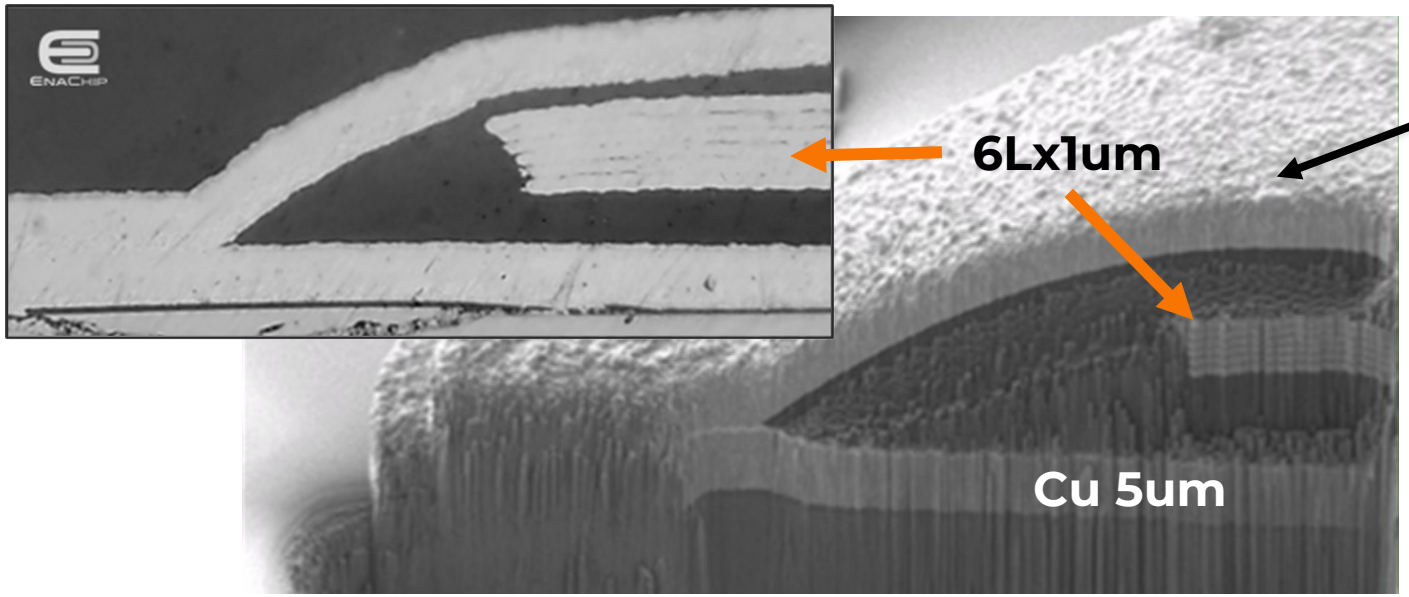


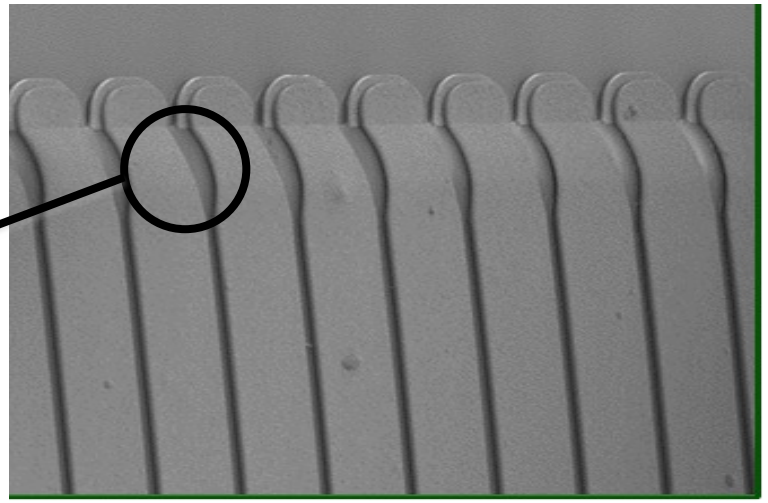
L=20-40nH die 2mm x 5mm

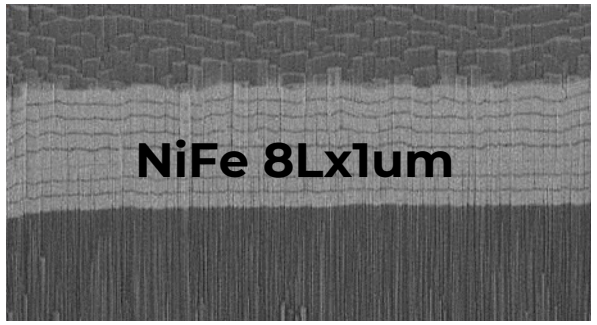


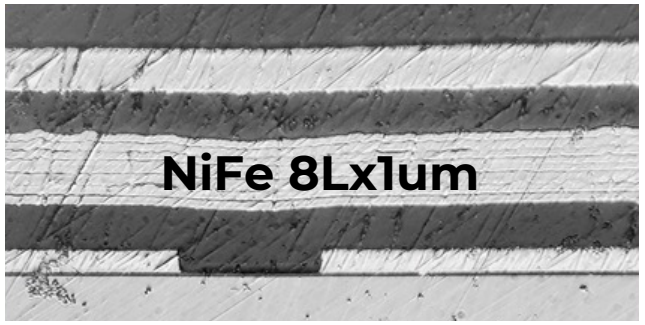
L=120-150nH die 1.7mm x 4.0mm

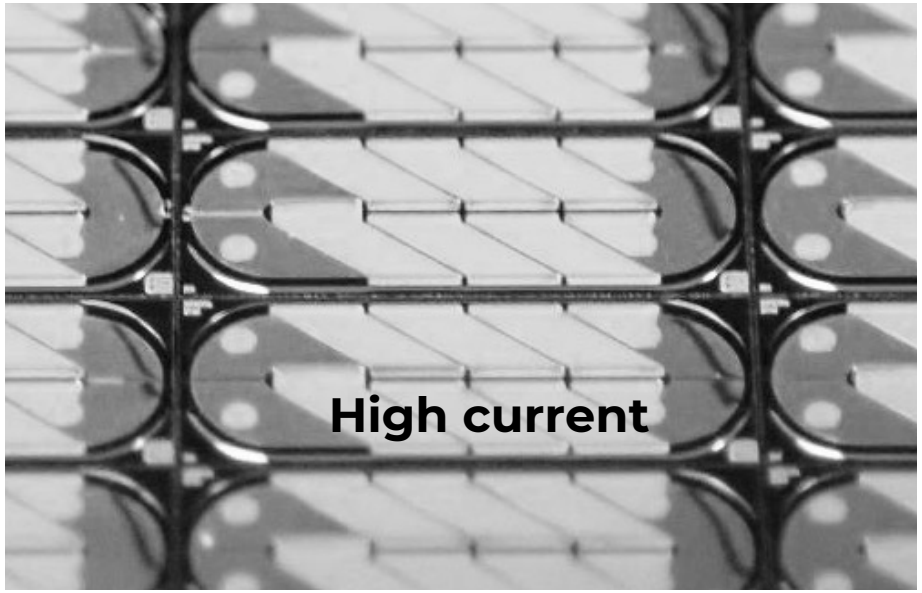
Device structure









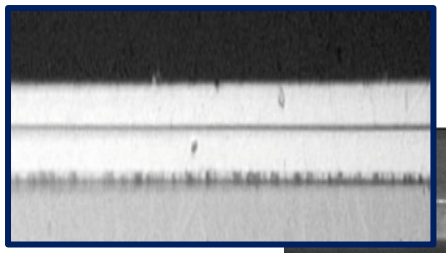


High Performance proprietary Mag. Alloys

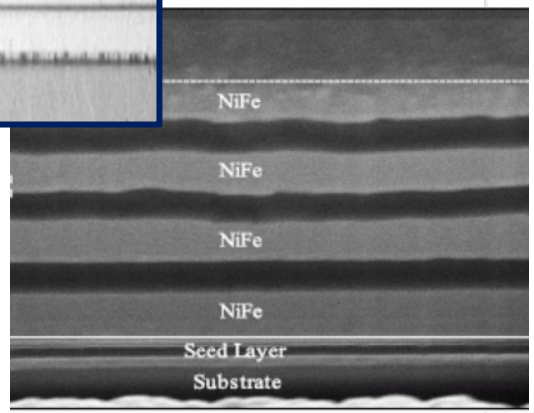
Ena**C**hip **A**lloy (**ECA**)

- Amorphous Electroplated
- 3x NiFe resistivity
- F_{sw} up to 30MHz

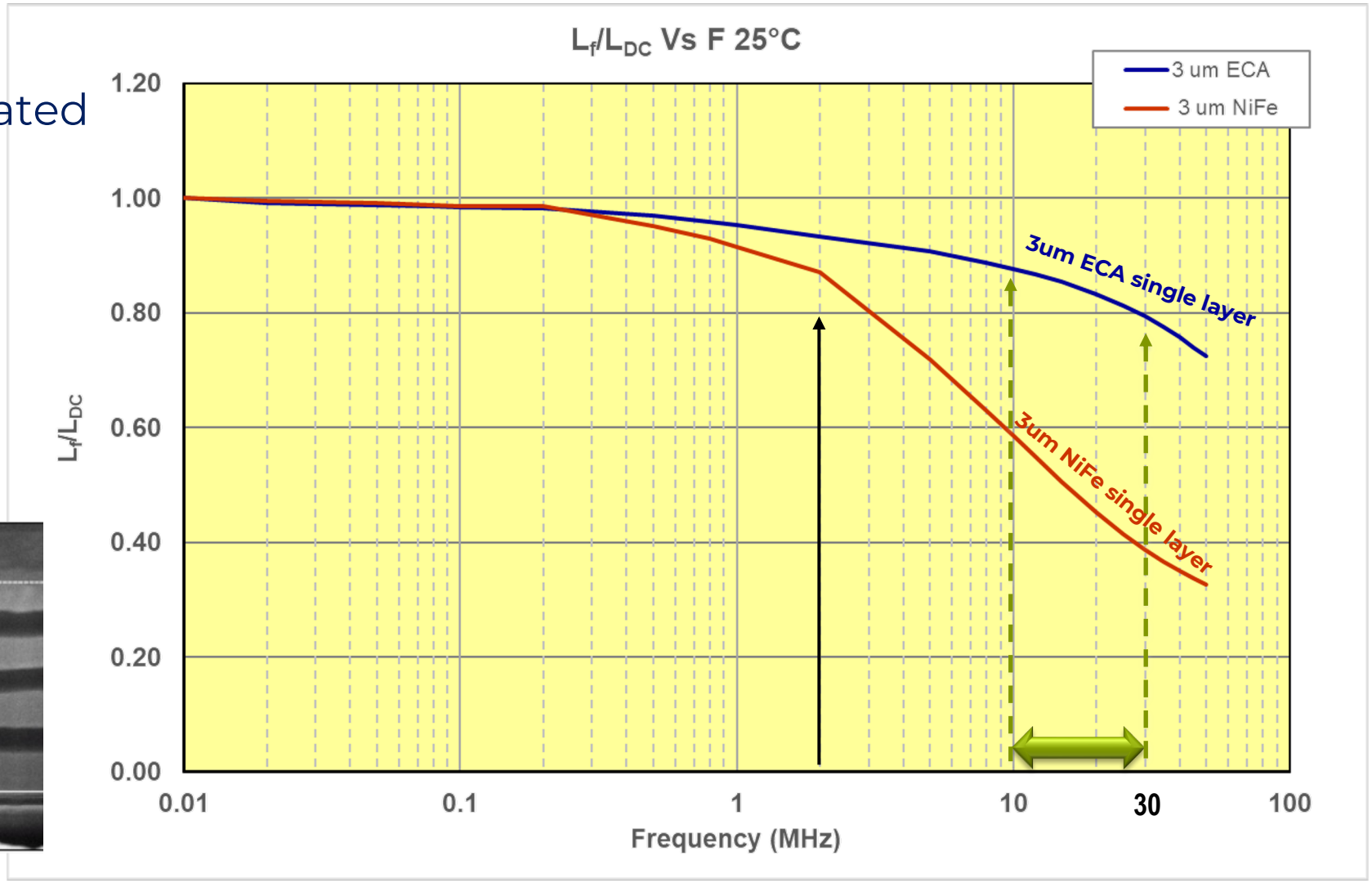
Using ECA we can build devices with less layers



ECA 2L



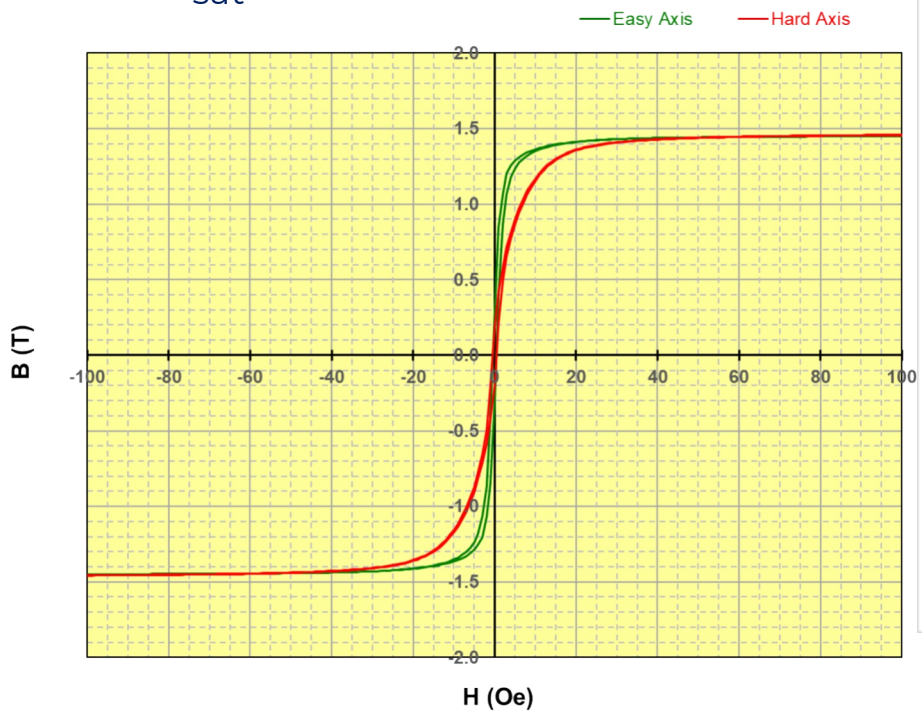
NiFe 4L



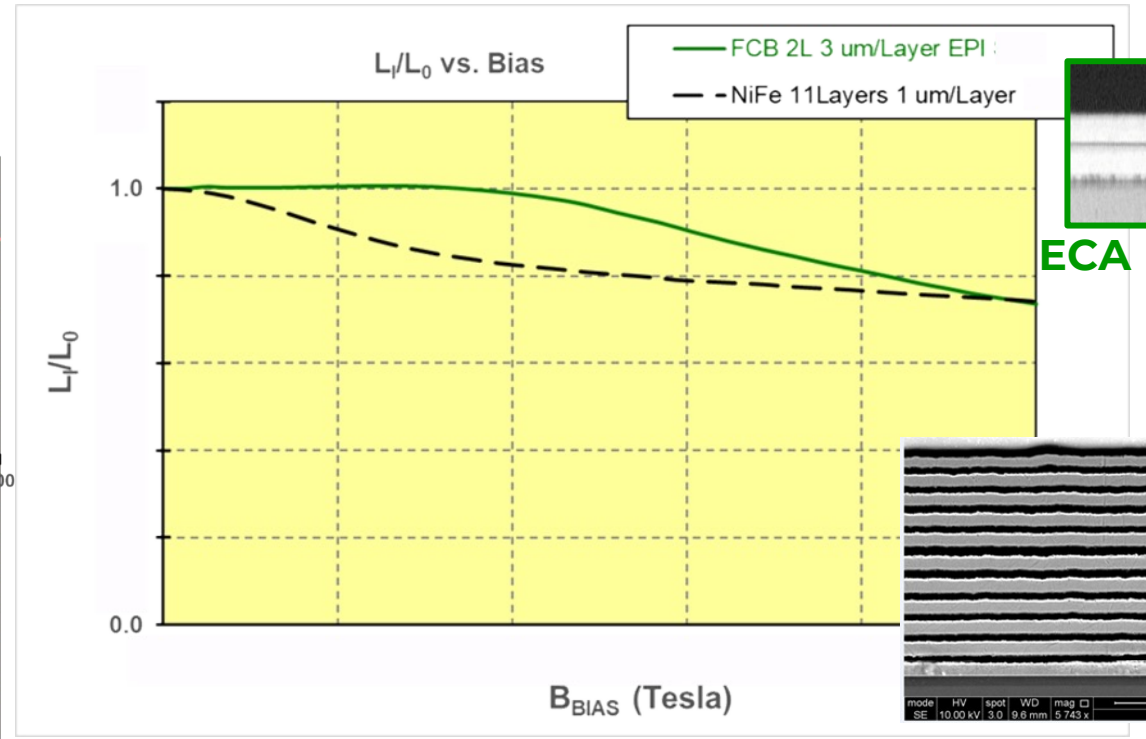
High Performance proprietary ECA alloy

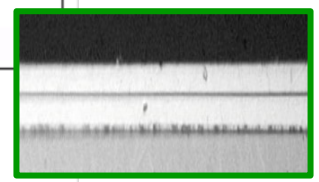
Ena**C**hip **A**lloy (**ECA**)

- Permeability up to 900
- $B_{sat} \geq 1.5$ T



ECA Bias operational range >> NiFe





ECA 2L/3µm ea

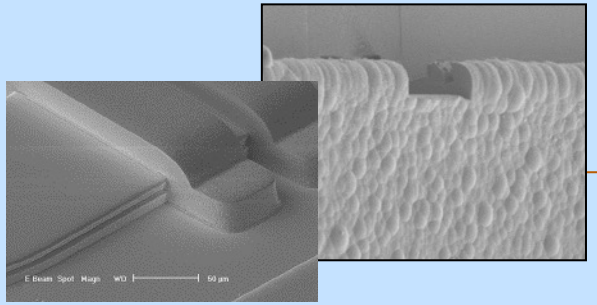
NiFe 11L/1µm ea

EnaChip Creates an Enabling Technology Platform

(MULTIPLE MARKET VERTICALS)

Post Process (BEOL-OSAT) compatible

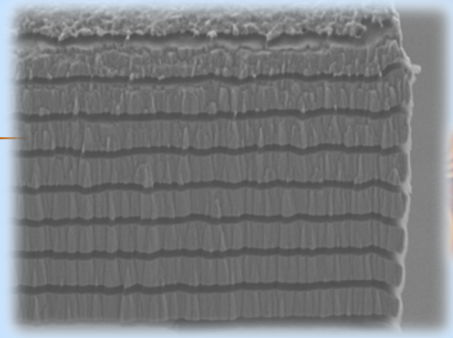
INDEPENDENT of Si node!

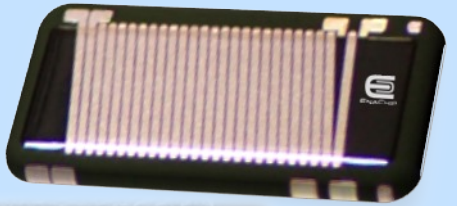


Unique high-performance magnetic materials

Leverages existing highest speed integrated electronic circuits

Innovative wafer fabrication processes





Unique Magnetic Alloys

- New Compositions of mater
- Unique formulations to meet performance
- Enachip Proprietary
- CMOS compatible

Miniaturization / Cost

Addressable Market Verticals

Voltage Regulation
- DC/DC Voltage Regulators
- Integrated Power Management IC
- LED Drivers

Magnetic Field Sensing
- Magnetic field -> Electric Signal

Power Harvesting
- RF→DC
- Solar -> DC/AC
- Mechanical -> DC/AC

Signal Conditioning
- Low Pass Filter
- Band Pass Filter
- Tuner
- RF Suppression (Beads)

Electromagnetic Actuation
- Electromagnetic Separation
  (Bio-medical devices POC Lab on Chip)
- Moving membranes
  (micro Pumps, micro Valves)
- Moving Beams
  (Reed switches, Relays)

Innovative Mfg. Processes
- Unique low-cost magnetic core laminations
- Copper windings
- Integrated circuit compatible

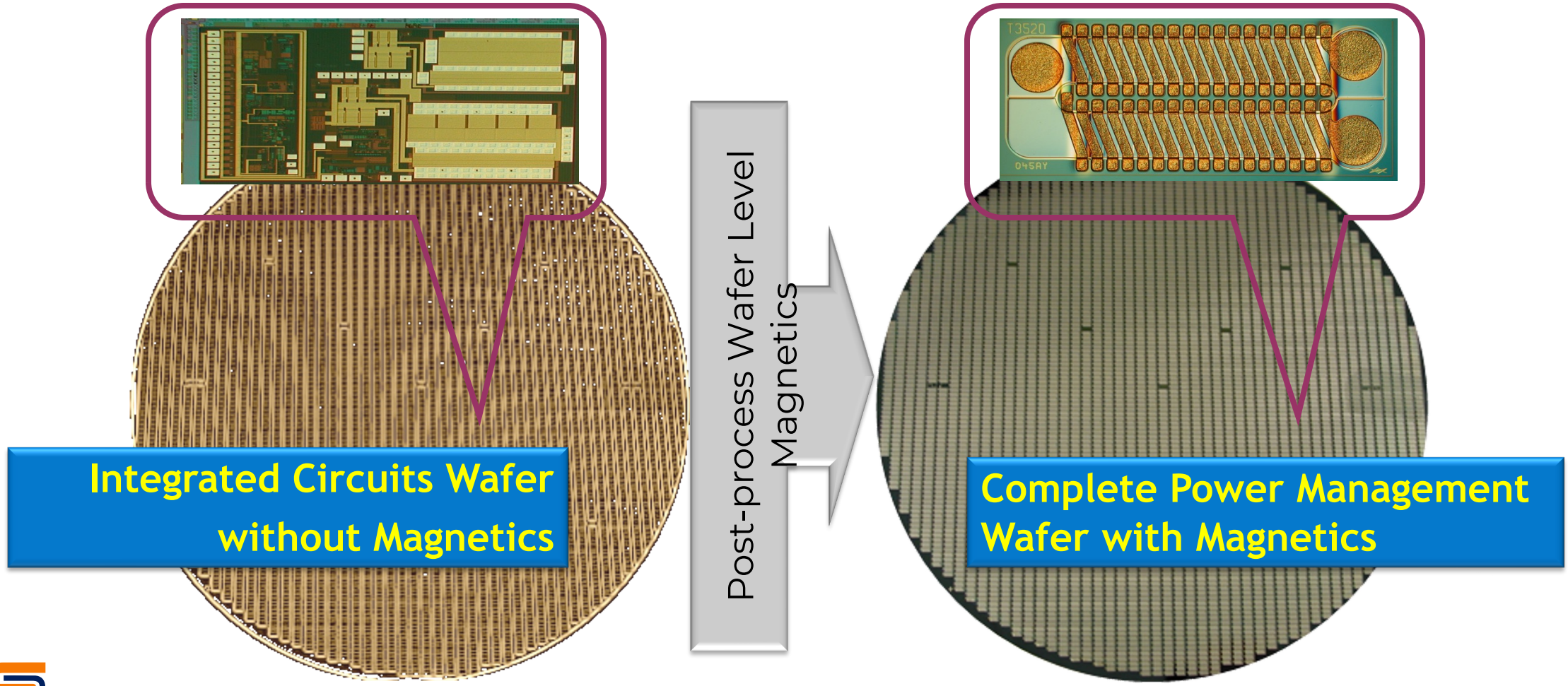
Performance / Cost

The advantage of being… Node-Agnostic

(Enachip's "Magnetic Functionality" can be post-processed on ***ANY substrate*** *from* ***ANY foundry*** *and* ***ANY node****)*

Controller+PFETs wafer

WLM post processed wafer

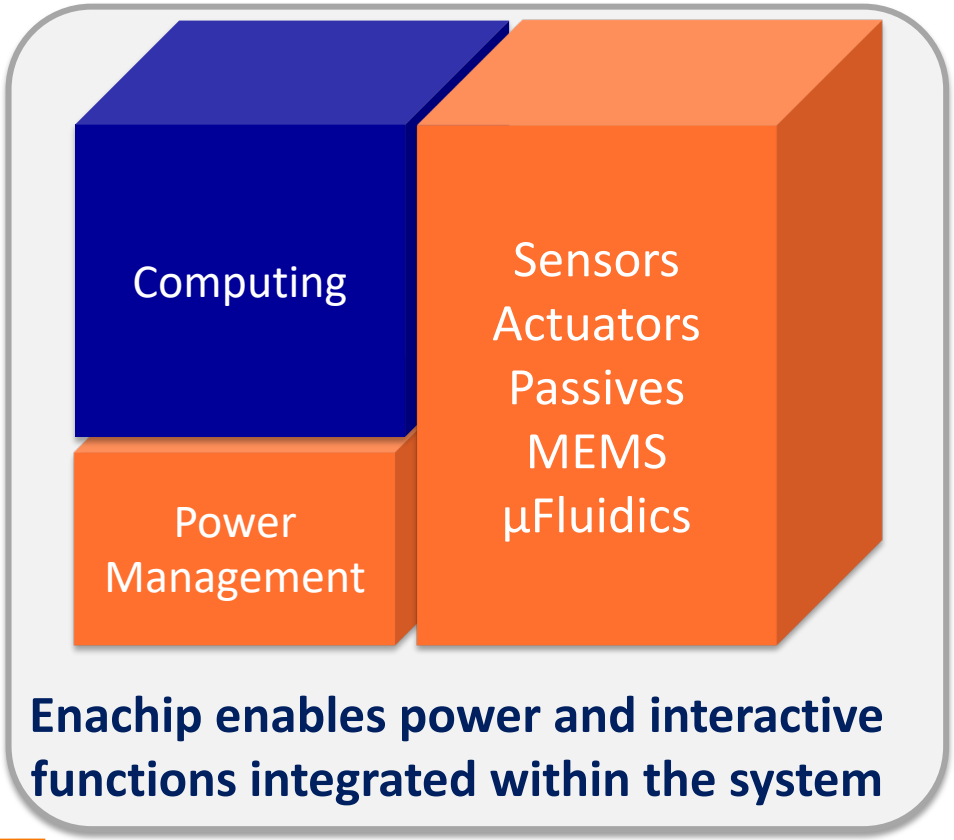


Smart Power Integration is needed in All Systems

WLM platform enables integration of power and interactive functions - **SoC**

Wafer Level Magnetic

System Integration at chip level

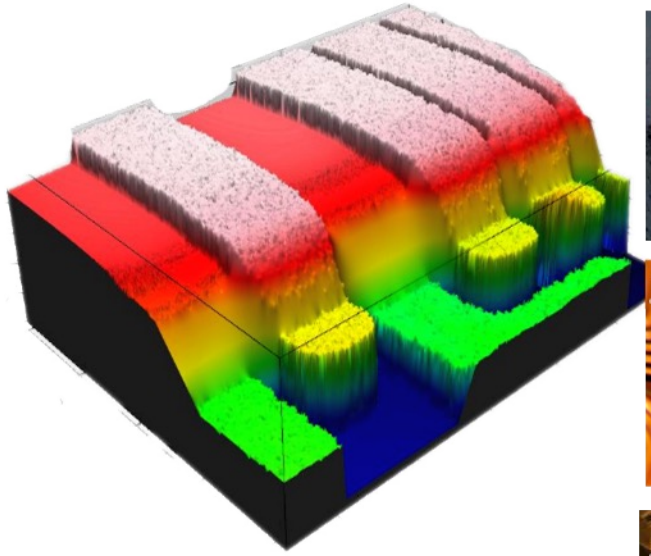


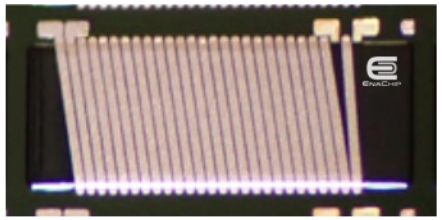
Enachip enables power and interactive functions integrated within the system

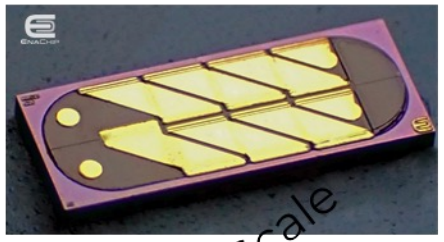
Devices are "talking" to environment and to the users

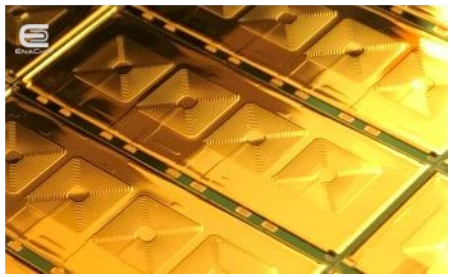
Device Examples

- Thick Cu toroid micro-inductors
- Multi-core toroids
- Spiral coils
- Electromagnets/Actuators
- Transformers
- Sensors









Walk away message:

First time demonstrated continuous electroplating of magnetic film and insulator sequentially

That enables:

Single mask thin film magnetic core laminations for high performance wafer level magnetics

Fast and Low cost BEOL – CMOS compatible simple manufacturing process with existing infrastructure

Performance enhancement by unique proprietary high performance electroplated magnetic alloys

Thank you!